(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 644 588 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 94113145.0

(22) Date of filing: 23.08.94

(51) Int. Cl.6: H01L 21/66, G01N 21/88

(30) Priority: 23.08.93 JP 231025/93

(43) Date of publication of application:
22.03.95 Bulletin 95/12

(84) Designated Contracting States:
DE FR GB IT NL

(71) Applicant: KOMATSU ELECTRONIC METALS CO., LTD
2612, Shinomiya
Hiratsuka-shi
Kangawa-ken (JP)

(72) Inventor: Uemura, Noriyuki
455-4 Kitanokubo
Odawara-shi,
Kanagawa-ken (JP)

Inventor: Motoura, Hisami
812-1, Shinomiya
Hiratsuka-shi,
Kanagawa-ken (JP)

Inventor: Nishimura, Masashi
4-20-1, Higashiyahata
Hiratsuka-shi,
Kanagawa-ken (JP)

Inventor: Kohno, Mitsuo
520, Ojiri
Hadano-shi,
Kanagawa-ken (JP)

(74) Representative: Strehl Schübel-Hopf Groening & Partner
Maximilianstrasse 54
D-80538 München (DE)

(54) Wafer with epitaxial layer having a low defect density.

(57) There is provided a high quality epitaxial wafer on which the density of microscopic defects in the epitaxial layer is reduced to keep the gate oxide integrity thereof sufficiently high and to reduce the leakage current at the P-N junction thereof when devices are incorporated, thereby improving the yield of such devices. In an epitaxial wafer obtained by forming an epitaxial layer on a substrate, the density of IR laser scatterers is 5×10^5 pieces/cm^3 or less throughout the epitaxial layer.

Fig. 1

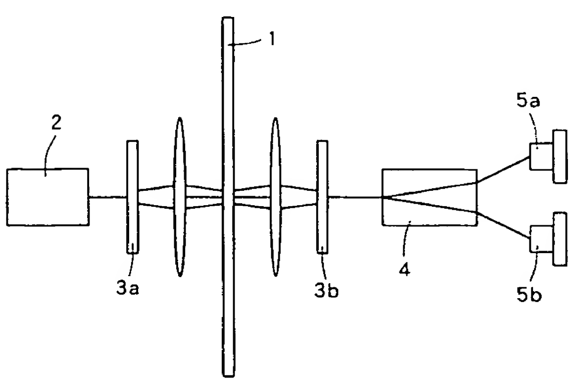
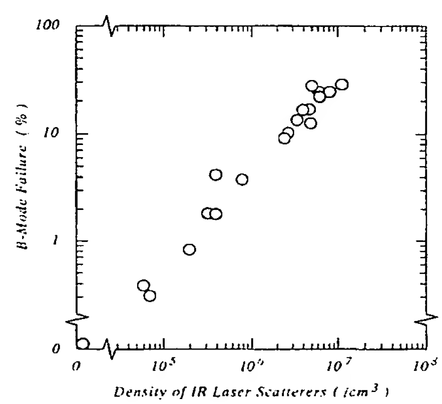


Fig. 2



BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an epitaxial wafer and, more particularly, to reduction of micro-defects associated with electrical characteristics of the wafer such as the gate oxide integrity (GOI) thereof.

Description of the Prior Art

Various devices are incorporated in a surface layer of an epitaxial wafer. In order that those devices properly electrically operate, the value of GOI thereof must be greater than a prescribed value, and a leakage current at a P-N junction formed in an epitaxial layer must be smaller than a prescribed value. However, factors affecting the electrical characteristics of the devices as described above have not been fully identified. Therefore, not a few such devices are judged to be defective because of GOI thereof smaller than the prescribed value, or the leakage current at the P-N junction thereof greater than the prescribed value. This has resulted in a decrease in the yield of such devices.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a high quality epitaxial wafer which is able to keep GOI sufficiently high, to reduce a leakage current at the P-N junction thereof when devices are incorporated, and to thereby improve the yield of such devices.

After researches for achieving the above-described object, the present inventors have turned attention to laser scatterers of a semiconductor wafer which produce scattered light when the wafer is irradiated by a IR (Infrared) laser on a surface of the wafer, and found that GOI of the wafer is deteriorated when there are many such IR laser scatterers. It has been also revealed that an increase in the number of the IR laser scatterers results in an increase in a leakage current at a P-N junction. Further, measurement has been done on the density of IR laser scatterers in an epitaxial wafer obtained by forming an epitaxial layer on a semiconductor wafer substrate, and it has been revealed that the epitaxial layer grows with succeeding a density of IR laser scatterers of the substrate at the side of the interface with the substrate, while the density goes down with departing from the interface and finally goes zero at the surface of the epitaxial layer. Thus, it has been revealed that such a profile of the IR laser scatterer density in the epitaxial layer causes deterioration in the electrical characteristics of active regions of devices, which finding led to the completion of the present invention.

According to a first aspect of the present invention, there is provided an epitaxial wafer comprising a substrate and an epitaxial layer formed on the substrate, wherein: the epitaxial layer has a density of IR laser scatterers of 5×10^5 pieces/cm^3 or less throughout the epitaxial layer. The substrate may be a wafer fabricated using the floating zone melting method, or a wafer fabricated using the Czochralski method wherein the pull rate is 0.6 mm/min. or slower. The substrate may also be a wafer which is fabricated according to the Czochralski method and is thereafter subjected to a heat treatment at 1330 to 1400 °C for 0.5 Hr or longer.

According to a second aspect of the present invention, there is provided an epitaxial wafer comprising a substrate and an epitaxial layer formed on the substrate, wherein: the epitaxial layer is comprised of a first and a second epitaxial sub-layers, the first epitaxial sub-layer is formed on the substrate, has the same conductivity type with the substrate, and has essentially same electrical resistivity with the substrate, and the second epitaxial sub-layer is formed on the first sub-layer, has a density of IR laser scatterers of 5×10^5 pieces/cm^3 or less, and has electrical resistivity higher than that of the first sub-layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a method of measuring the density of IR laser scatterers.

Fig. 2 illustrates the relationship between the density of IR laser scatterers in a surface region and B-mode failure.

Fig. 3 illustrates the relationship between the density of IR laser scatterers in a surface region and C-mode yield.

Fig. 4 illustrates the density profile of IR laser scatterers in the direction of depth of an epitaxial wafer.

Fig. 5 illustrates a region having less defects and a transition region relative to the thickness of an epitaxial layer.

Fig. 6 illustrates the relationship between the density of IR laser scatterers in a surface region and the temperature of a heat treatment.

Fig. 7 illustrates the density profile of IR laser scatterers in the direction of depth of an epitaxial wafer obtained using a vertical scattering method and a transmission scattering method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the present invention will now be described. Silicon wafer samples were produced by fabricating a single crystal silicon ingot using the pull method, i.e., the Czochralski method, and by performing processes of slicing, lapping, chamfering and chemical polishing thereon. The specifications of the samples were as follows.

Diameter: 6 inches

Crystal Axis: ⟨100⟩

P-type

Boron-doped

Resistivity: 10 to 20 Ωcm

Concentration of Oxygen: 12 to 15 X 10^{17} atoms/cm^3 The above specification are shown in accordance with the Annual Book of ASTM Standards of the year of 1979. The measurements shown in the following description are based on this specification. The density of IR laser scatterers was measured on the samples and GOI was measured on MOS capacitors which have been actually fabricated using the samples.

Fig. 1 shows a device for measuring the density of IR laser scatterers in the above-described sample. A laser beam having a wavelength of 1.3 µm is vertically directed from a laser source 2 to the surface of a silicon wafer 1 through a first prism 3a and is focused on the surface of the silicon wafer 1 or in the interior thereof. The wafer 1 is then slid to scan a plurality of arbitrarily determined points on the surface of the wafer 1 or in the interior thereof. The laser beam which has passed through the wafer 1 is led to an analyzer 4 through a second prism 3b and a phase shift of the beam is detected using two detectors 5a and 5b. When the beam impinges upon a defect in the wafer 1, there will be a slight shift in the phase thereof. Thus, the defect can be detected by detecting the phase shift.

Fig. 2 shows the relationship between the density of IR laser scatterers in the vicinity of the surface of the silicon wafer 1, that is , 0 to 3 µm in depth, and the proportion of B-mode failure wherein the breakdown voltage is in the range between 3 MV/cm and 8 MV/cm. It will be appreciated from this figure that there is significant correlation between the density of IR laser scatterers and the B-mode failure, i.e., the B-mode failure increases with an increase in the density of IR laser scatterers. Fig. 3 shows the relationship between the density of IR laser scatterers and the proportion of C-mode yield wherein the breakdown voltage is 8 MV/cm or higher. It will be appreciated from this figure that the C-mode yield decreases with an increase in the density of IR laser scatterers.

Specifically, the C-mode yield must be 95 % or higher in general with respect to the GOI. It is therefore apparent from Fig. 3 that the density of IR laser scatterers must be approximately 5 X 10^5 pieces/cm^3 or less. Since this equally applies to an epitaxial wafer, the density of IR laser scatterers must be 5 X 10^5 pieces/cm^3 or less to obtain the epitaxial wafer having a sufficiently high GOI.

Fig. 4 shows the measurement results of IR laser scatterer density in the direction of the depth of epitaxial wafers obtained by respectively forming epitaxial layers (written as "Epi" in drawing) having thicknesses of 10 µm, 20 µm, 30 µm and 60 µm on silicon wafer substrates fabricated using the Czochralski method (written as "CZ" in drawing), and an epitaxial wafer obtained by forming an epitaxial layer having a thickness of 10 µm on a silicon wafer substrate fabricated using the floating zone melting method (written as "FZ" in drawing). On the epitaxial wafers obtained by forming epitaxial layers on the silicon wafer substrates fabricated using the Czochralski method, the epitaxial layers grow with IR laser scatterers in a density equal to that of the substrates at the side of the interface with the substrates, while the density of the IR laser scatterers is zero at the surfaces of the epitaxial layers. Specifically, in this embodiment, the density of IR laser scatterers in the substrate is about 1 X 10^6 pieces/cm^3 while the density of IR laser scatterers is gradually reduced from 1 X 10^6 pieces/cm^3 to 5 X 10^5 pieces/cm^3 in a transition region at the substrate side of the epitaxial layer, and further reduced to zero. However, for a wafer similarly fabricated using the Czochralski method at a slow pull rate of 0.6 mm/min. having an epitaxial layer of 60 µm formed thereon, the density of IR laser scatterers is zero regardless of the depth from the surface of the wafer.

Fig. 5 illustrates the same results from a different point of view and shows a range wherein the density of IR laser scatterers is zero, and a range wherein the density is 5 X 10^5 pieces/cm^3 or less. It is apparent from this figure that the IR laser scatterer density is not necessarily zero throughout an epitaxial layer nor 5 X 10^5 pieces/cm^3 or less throughout the layer.

Returning back to Fig. 4 to see an epitaxial wafer which is obtained by forming an epitaxial layer on a silicon wafer substrate fabricated using the floating zone melting method, as the IR laser scatterer density is zero in the substrate in this case, the IR laser scatterer density in the epitaxial layer is also zero.

As previously described, the density of IR laser scatterers must be 5 X 10^5 pieces/cm^3 or less in order to get an epitaxial wafer having a sufficiently high GOI. In order that the density of IR laser scatterers is 5 X 10^5 pieces/cm^3 or less throughout

an epitaxial layer, the IR laser scatterer density must be 5 X 10^5 pieces/cm^3 or less in the substrate as apparent from Fig. 4. As far as the inventors have studied, there has been no epitaxial wafer wherein the density of IR laser scatterers is 5 X 10^5 pieces/cm^3 or less throughout the epitaxial layer thereof.

The above-described results on IR laser scatterers are based on an evaluation made in accordance with the transmission scattering method. But the same tendency has been observed, as shown in Fig. 7, in an evaluation made in accordance with the vertical scattering method using a laser beam having a wavelength of 1.06 μm. However, the measurement is difficult by the vertical scattering method in the vicinity of the surface of a wafer, that is, 0 to 10 μm in depth, due to scattered light at the surface of the wafer. Therefore, the result obtained using the transmission scattering method has been described, wherein measurement can be made on all parts of a wafer.

As a first means for reducing the density of IR laser scatterers in a substrate to 5 X 10^5 pieces/cm^3 or less, the substrate can be fabricated using the floating zone melting method as shown in Fig. 4. As a second means for reducing the density of IR laser scatterers to 5 X 10^5 pieces/cm^3 or less, the Czochralski method may be employed with the pull rate reduced to 0.6 mm/min. or less. However, this method has a problem in that it is poor from the viewpoint of productivity in growing crystals. As a third means, a description will be made on a method wherein a heat treatment is performed on single crystal silicon fabricated using the Czochralski method at a normal pull rate.

Fig. 6 shows the density of IR laser scatterers in the vicinity of the surface of the silicon wafer, that is, 0 to 3 μm in depth, under varied conditions for the heat treatment. As shown in this figure, there are IR laser scatterers in a density on the order of 3 X 10^6 pieces/cm^3 in this embodiment when no heat treatment is performed. It will be understood that this IR laser scatterer density remains almost unchanged even if the heat treatment is performed at temperatures up to about 1300 °C , or the heat treatment is performed for a long time, which means that the IR laser scatterers are very stable. However, if the temperature for the heat treatment is increased beyond approximately 1330 °C , the IR laser scatterers are almost completely eliminated after at least 0.5 hours of such heat treatment. Thus, the IR laser scatterers can be substantially completely eliminated by performing the heat treatment at a temperature in the range between 1330 and 1400 °C , considering the melting point of silicon, for 0.5 hours or longer. And by forming an epitaxial layer on a substrate which has been subjected to such heat treatment, it is possible to obtain an epitaxial wafer in which the yield is sufficiently high with respect to the GOI.

There is no relationship between the processing of a silicon ingot into a silicon wafer and the heat treatment at 1330 to 1400 °C for 0.5 hours or longer. Therefore, the heat treatment may be performed not only after processing an ingot into a silicon wafer but also on a silicon ingot before processing which may be then processed into a silicon wafer. As to the device for such a heat treatment, a container to be exclusively used for the heat treatment may be employed. Alternatively, a pulling device itself may be used as a heating furnace, which method is advantageous especially when the heat treatment is performed on a silicon ingot.

Besides the above-described embodiment, epitaxial growth was observed on a crystal of specifications as follows, which is obtained using the Czochralski method at a pull rate of 0.6 mm/min. or slower.

Diameter: 6 inches
Crystal axis: ⟨100⟩
P-type
Boron-doped
Resistivity: 0.01 to 0.02 Ωcm
Concentration of Oxygen: 12 to 15 X 10^{17} atoms/cm^3 In this case, the number of IR laser scatterers in the epitaxial layer was also 5 X 10^5 pieces/cm^3 or less and similar effects were obtained with respect to electrical characteristics such as GOI and the leakage current at the P-N junction.

Further, epitaxial growth was observed on a crystal of specifications as follows, which is obtained using the Czochralski method at a normal pull rate and is performed with a heat treatment at a temperature in the rage between 1330 and 1400 °C for 0.5 hours or longer.

Diameter: 6 inches
Crystal axis: ⟨100⟩
N-type
Antimony-doped
Resistivity: 0.01 to 0.02 Ωcm
Concentration of Oxygen: 13 to 16 X 10^{17} atoms/cm^3 Again, the number of IR laser scatterers in the epitaxial layer was 5 X 10^5 pieces/cm^3 or less and similar effects were obtained with respect to electrical characteristics such as GOI and the leakage current at the P-N junction.

For an epitaxial wafer substrate having low resistivity on the order of 0.01 Ωcm, an improvement can be expected in anti-latch-up characteristics after formation of devices. Specifically, since the present invention suppresses the IR laser scatterers in the epitaxial layer which grow with succeeding that of the epitaxial wafer substrate, the thickness of the epitaxial layer can be reduced down to the thickness of the device active layer, so

that an advantage is obtained, from an industrial point of view, in the improved anti-latch-up characteristics.

Next, as previously described, as for an epitaxial wafer obtained by forming an epitaxial layer on a silicon wafer fabricated using the Czochralski method, there exists a transition region at the side of the epitaxial layer closer to the substrate. Therefore, only a layer closer to the surface than the transition region can be used for an active region. In this case, the anti-latch-up characteristics of the devices formed can be improved by making the electrical resistance of the used layer smaller than that of the transition region.

Specifically, assume that the transition region and the used layer are referred to as a first sub-layer and a second sub-layer, respectively. Then, the thickness of the second sub-layer serving as the used layer is first decided; the overall thickness of the epitaxial layer required in order that the density of IR laser scatterers in the second sub-layer is 5 X 10^5 pieces/cm^3 or less, is obtained according to Fig. 5; and the thickness of the first sub-layer is obtained by subtracting the thickness of the second sub-layer from the overall thickness. Thereafter, if the substrate, for example, is Boron-doped and has an electrical resistance of 0.01 to 0.02 Ωcm, the first sub-layer is formed as to also be Boron-doped with an electrical resistance in the order of 0.01 to 0.02 Ωcm. And the second sub-layer is provided with an electrical resistance of, for example, 5 to 10 Ωcm. Since this makes the density of IR laser scatterers in the second epitaxial sub-layer low, it is possible to minimize the thickness of such epitaxial layers and consequently to provide an epitaxial wafer having excellent anti-latch-up characteristics.

As described above, the present invention makes it possible to promote improvements in electrical characteristics such as a GOI and a leakage current at a P-N junction and to thereby obtain an epitaxial wafer having excellent anti-latch-up characteristics by reducing the density of IR laser scatterers in an epitaxial layer to 5 X 10^5 pieces/cm^3 or less. Although the embodiments of the present invention have been described above, various modifications are possible without departing from the spirit of the invention which is defined solely in the appended claims.

Claims

1. An epitaxial wafer comprising a substrate and an epitaxial layer formed on said substrate said epitaxial layer having a density of IR laser scatterers of 5 x 10^5 pieces/cm^3 or less throughout said epitaxial layer.

2. The epitaxial waver of claim 1, wherein said substrate is a wafer fabricated using a floating zone melting method.

3. The epitaxial waver of claim 1, wherein said substrate is a wafer fabricated using the Czochralski method at a pull rate of 0.6 mm/min or slower.

4. The epitaxial waver of claim 1, wherein said substrate is a wafer which has been subjected to a heat process at a temperature in the range between 1330 and 1400 °C for 0.5 hours or longer after being fabricated using the Czochralski method.

5. An epitaxial wafer comprising a substrate and an epitaxial layer formed on said substrate, said epitaxial layer including a first epitaxial sub-layer formed on said substrate, and having the same conductivity type and essentially the same electrical resistivity as the substrate, and

a second epitaxial sub-layer formed on said first sublayer and having a density of IR laser scatterers of 5 x 10^5 pieces/cm^3 or less and an electrical resistivity higher than that of said first sub-layer.

6. A process of fabricating an epitaxial wafer by

forming a substrate by floating-zone melting or by the Czochralski method at a pull rate of 0.6 mm/min or less,

forming on said substrate an epitaxial layer having a density of IR laser scatterers of 5 x 10^5 cm^{-3} or less.

7. The process of claim 6, wherein the substrate formed by using the Czochralski method is heat-treated at a temperature between 1330 and 1400 °C for at least 0.5 hours.

8. The process of claim 6 or 7, wherein said epitaxial layer is produced by

forming on said substrate a first epitaxial sub-layer of the same conductivity type and substantially the same electrical resistivity as the substrate, and

forming on said first sub-layer a second epitaxial sublayer having a density of IR laser scatterers of 5 x 10^5 cm^{-3} or less and a higher electrical resistivity than the first sub-layer.

Fig. 1

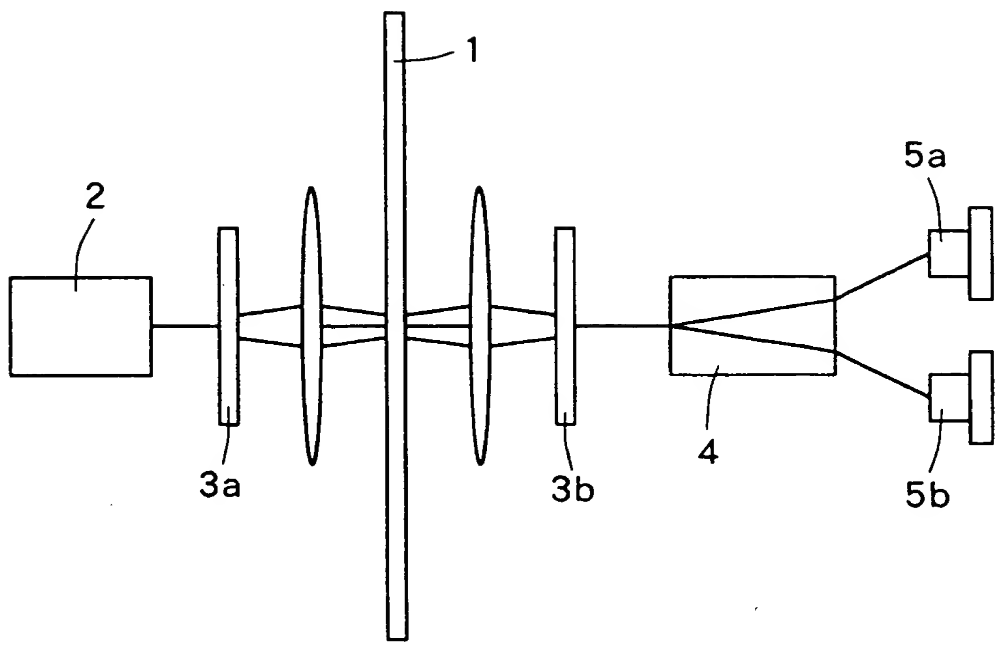


Fig. 2

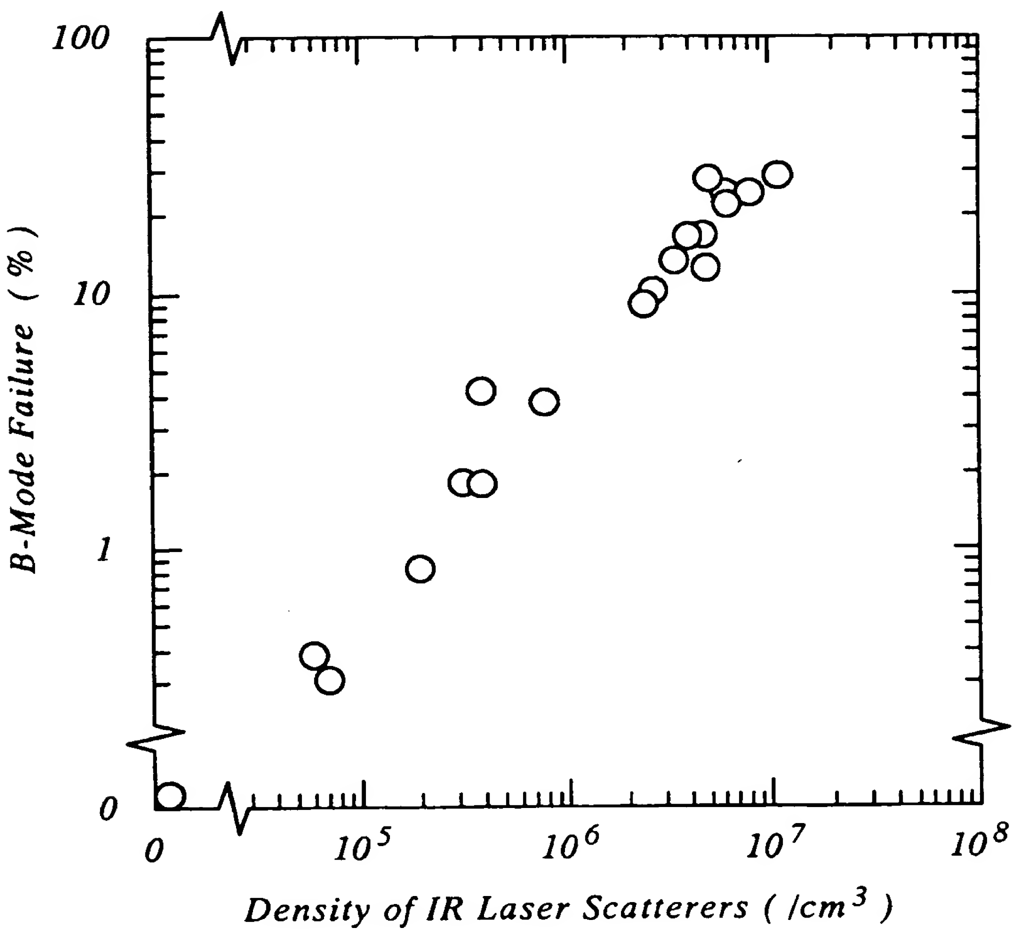

100
10
1
0
B-Mode Failure (%)
0
10^5
10^6
10^7
10^8
Density of IR Laser Scatterers (/cm^3)

Fig. 3

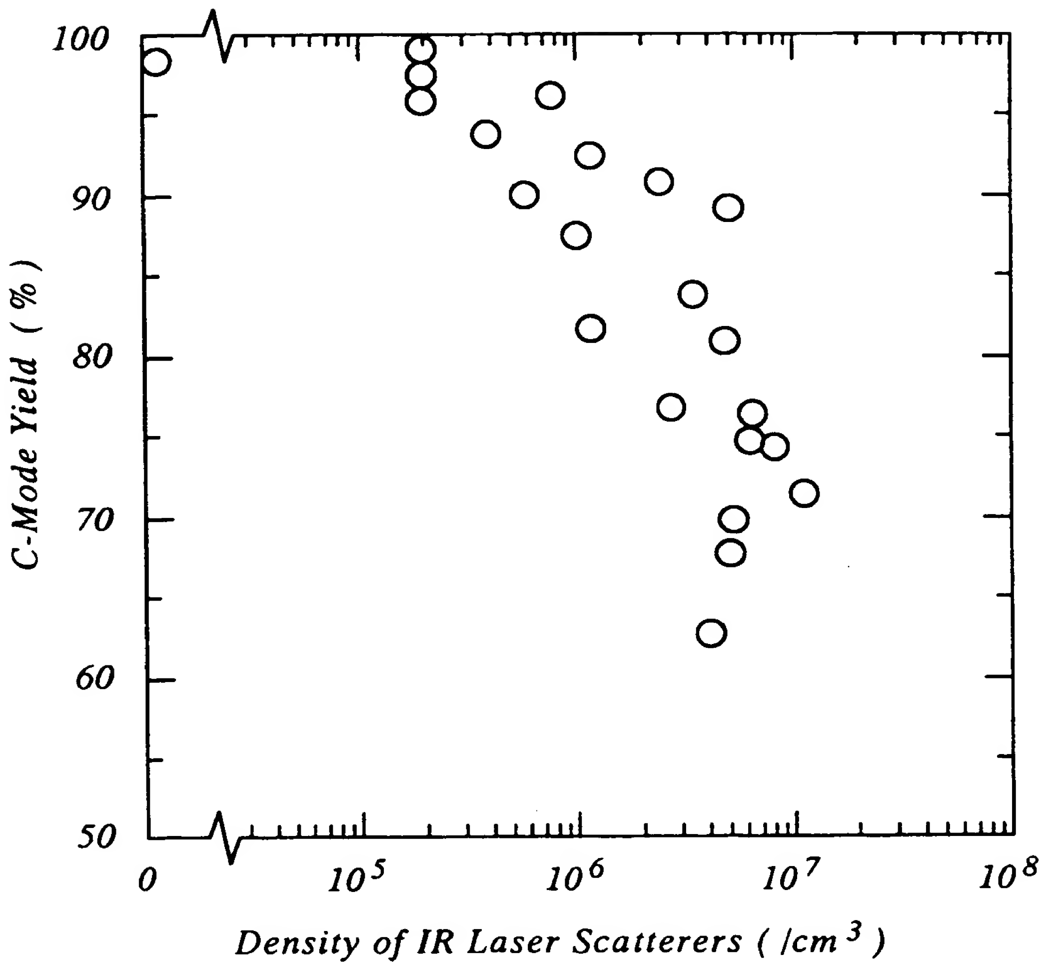

100
90
80
70
60
50
C-Mode Yield (%)
0
10^5
10^6
10^7
10^8
Density of IR Laser Scatterers (/cm ^{3})

Fig. 4

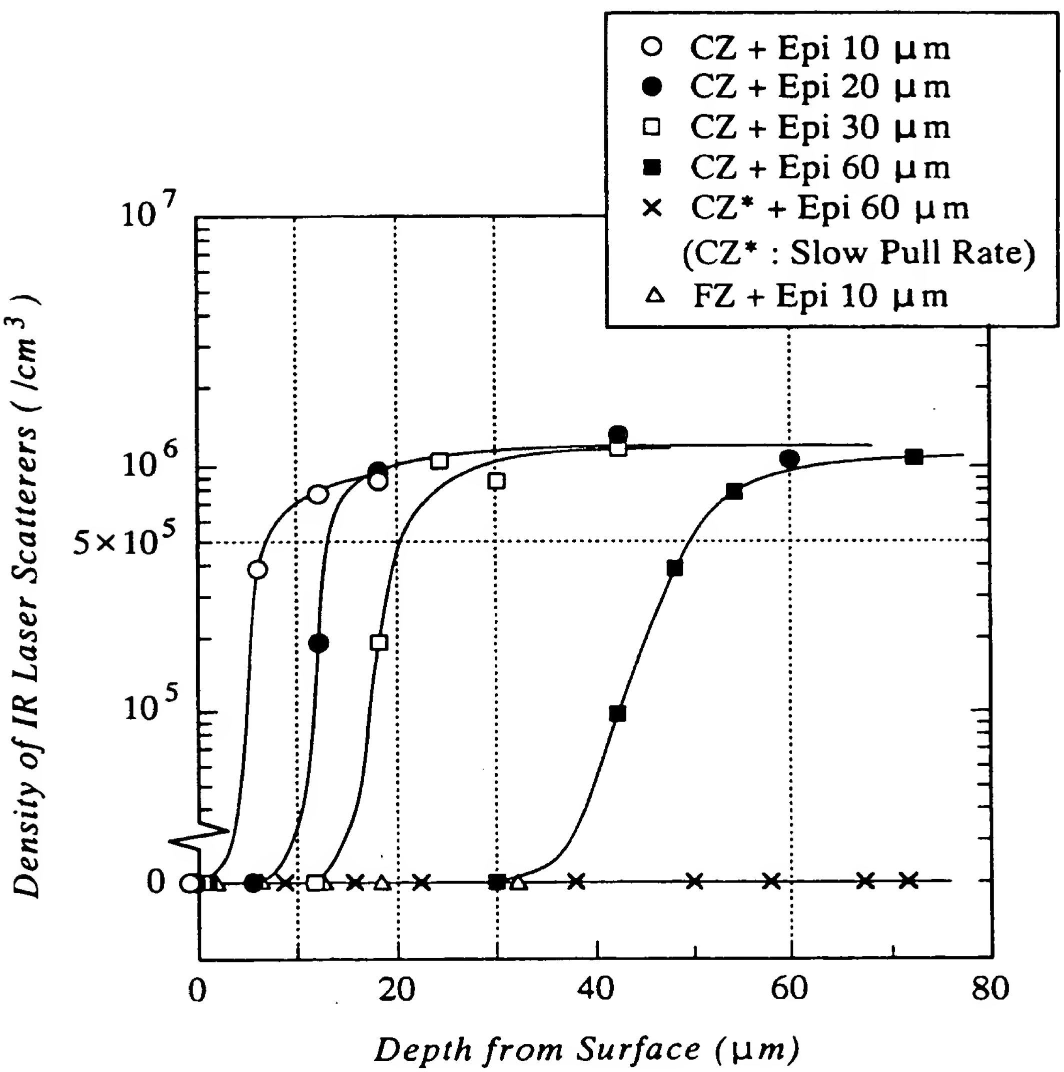

CZ + Epi 10 μm
CZ + Epi 20 μm
CZ + Epi 30 μm
CZ + Epi 60 μm
CZ* + Epi 60 μm
(CZ* : Slow Pull Rate)
FZ + Epi 10 μm
10^7
10^6
5×10^5
10^5
0
Density of IR Laser Scatterers (/cm^3)
0
20
40
60
80
Depth from Surface (μm)

Fig. 5

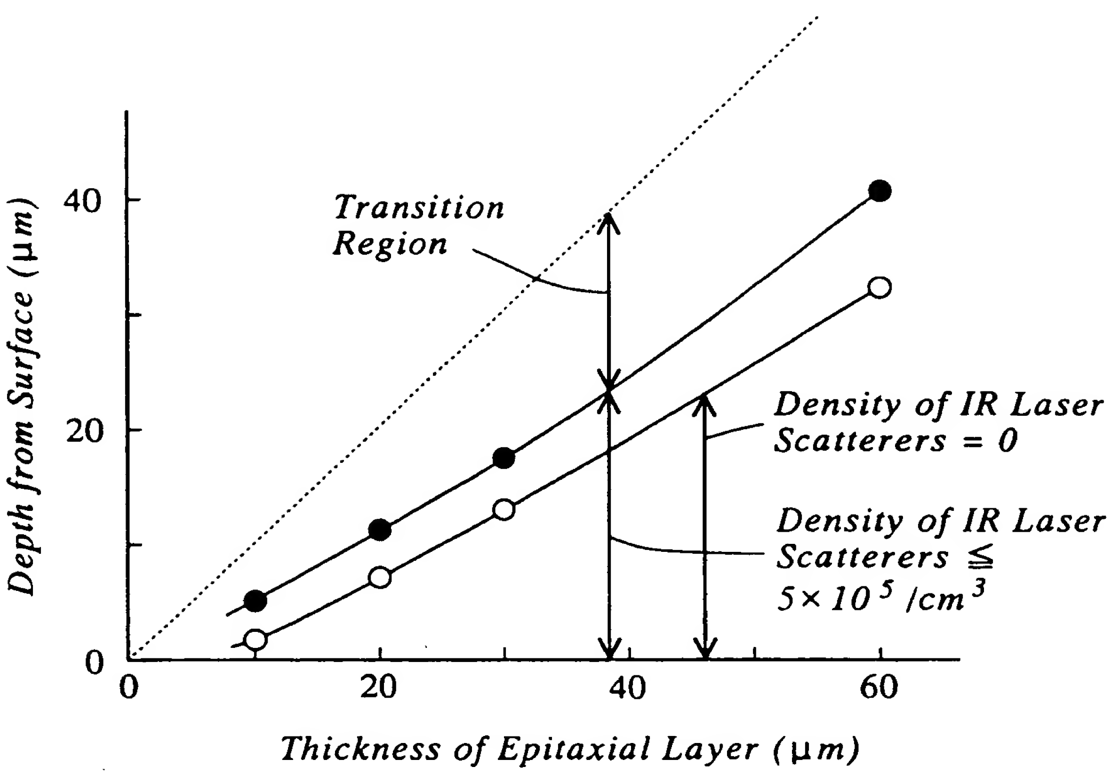

Depth from Surface (μm)
40
20
0
Transition
Region
Density of IR Laser
Scatterers = 0
Density of IR Laser
Scatterers ≦
5× 10^5 /cm^3
0
20
40
60
Thickness of Epitaxial Layer (μm)

Fig. 6

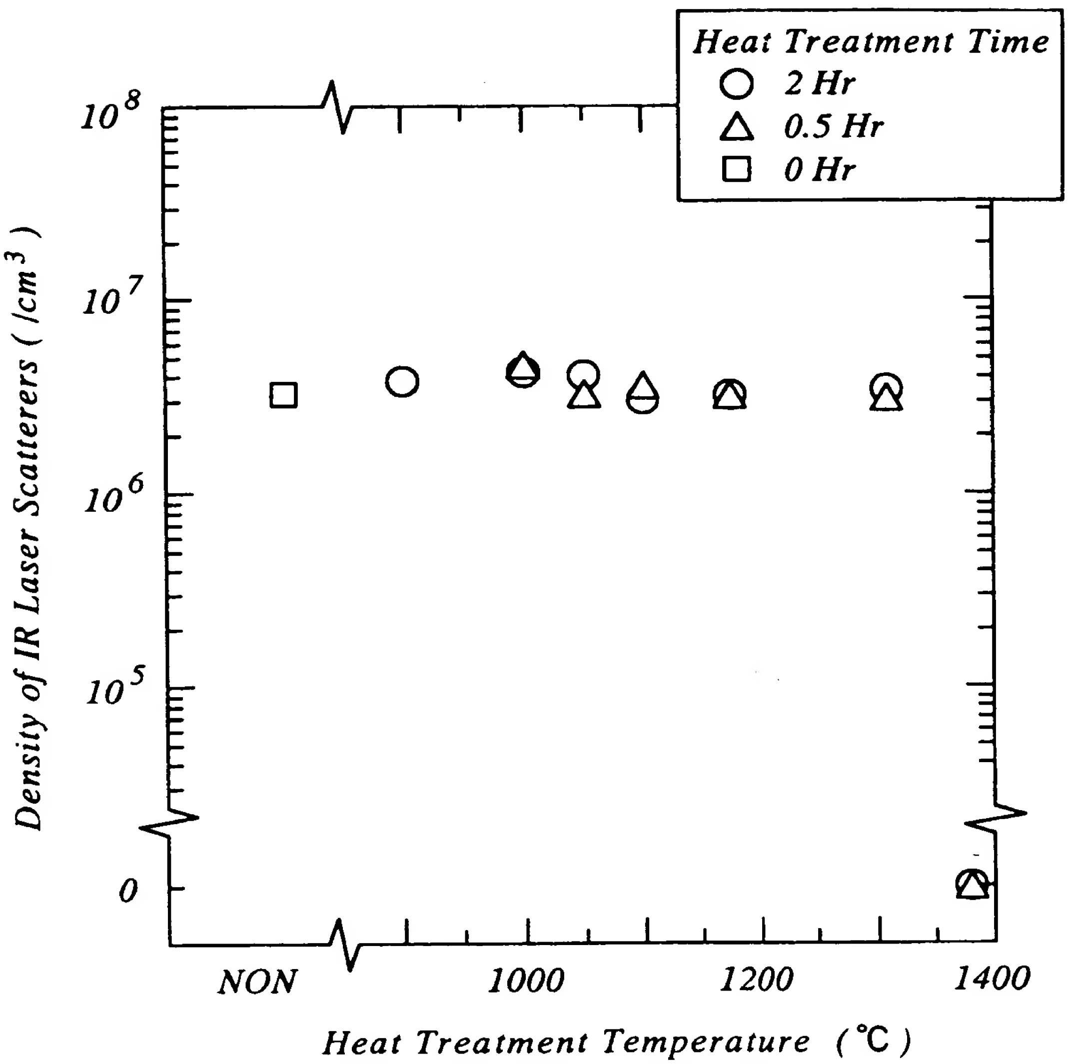
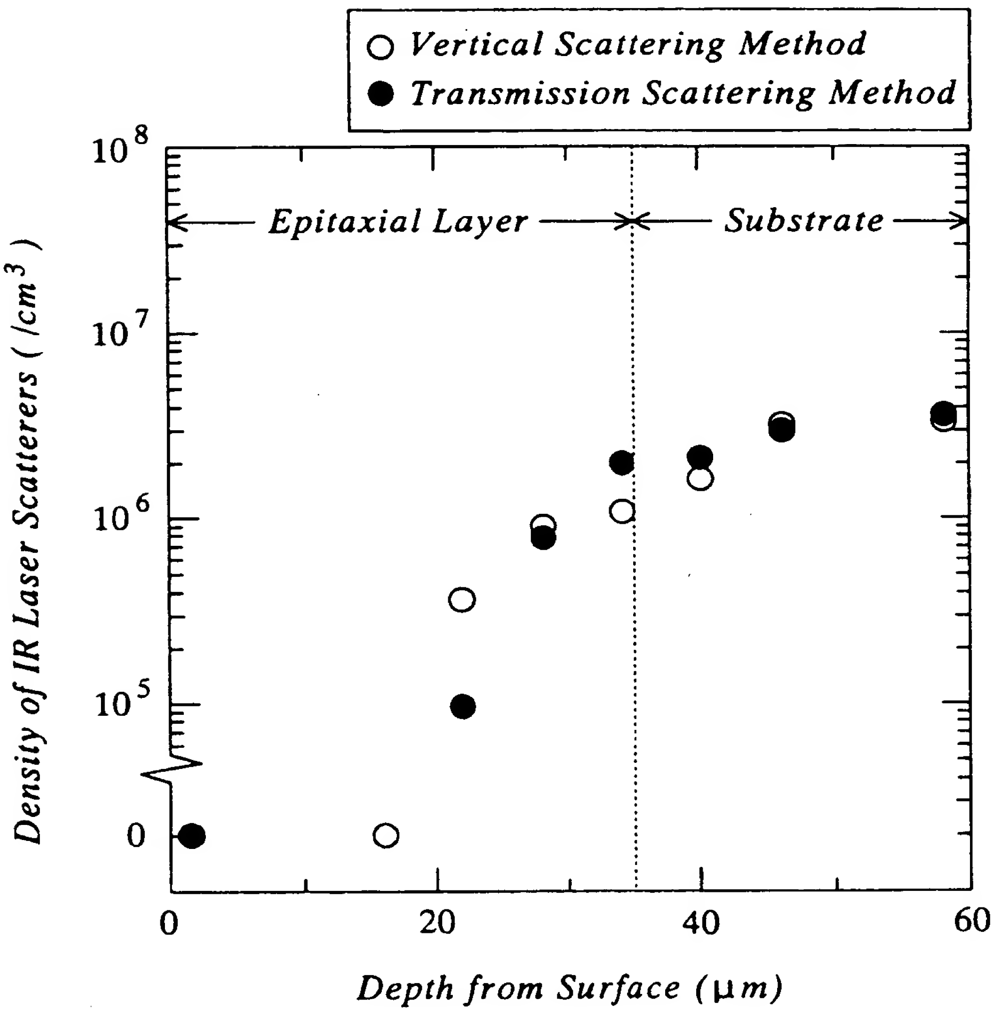

Heat Treatment Time
2 Hr
0.5 Hr
0 Hr
10^8
10^7
10^6
10^5
0
Density of IR Laser Scatterers (/cm^3)
NON
1000
1200
1400
Heat Treatment Temperature (℃)

Fig. 7


Vertical Scattering Method
Transmission Scattering Method
Epitaxial Layer
Substrate
Density of IR Laser Scatterers (/cm³)
10⁸
10⁷
10⁶
10⁵
0
0
20
40
60
Depth from Surface (μm)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 3145

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	JOURNAL OF CRYSTAL GROWTH., vol.114, no.1/2, October 1991, AMSTERDAM NL pages 64 - 70 L. TAIJING ET AL * the whole document *	1,3,6	H01L21/66 G01N21/88
X	EP-A-0 468 213 (TOSHIBA) * page 3, line 29 - page 4, line 3 * * page 6, line 7 - line 28; figures *	1,3,6	
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 135 (E-604) 23 April 1988 & JP-A-62 261 138 (TOSHIBA CORP.) 13 November 1987 * abstract *	1,6	
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 263 (P-886) 19 June 1989 & JP-A-01 057 154 (NIKON CORP.) 3 March 1989 * abstract *	1,6	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, vol.B68, no.1/4, May 1992, AMSTERDAM NL pages 190 - 201 R. FLAGMEYER * the whole document *	1,5,6,8	H01L G01N
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol.138, no.6, June 1991, MANCHESTER, NEW HAMPSHIRE US pages 1784 - 1787 H. SHIRAI * the whole document *	1,6	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 December 1994	Roussel, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

THIS PAGE BLANK (USPTO)